Methods of Using Commercial Electromagnetic Simulators for Microwave and Millimeter-Wave Circuit Design and Optimization

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(Invited Paper)

Abstract—Efficient utilization of commercial electromagnetic (EM) simulators for design and optimization of microwave (MW) and millimeter-wave (MMW) circuits is achieved by classifying design problems into three categories—characterization of circuit elements, optimization of circuit elements, and creation of circuit element libraries such as scalable libraries. Practical aspects of the methods are illustrated by several examples. An equivalent circuit extraction technique suitable for n-port coupled structures is provided. The derived equivalent circuit is useful for extrapolating data, optimization, and deriving scalable models.

Index Terms—Circuit optimization, electromagnetic analysis, microwave circuits, passive circuits.

I. INTRODUCTION

IN THE LAST few years, there has been a significant improvement in both computer resources (in terms of central processing unit (CPU) speed and reduced random-access memory (RAM) prices) and electromagnetic (EM) simulation software [1] so that use of commercial EM simulators has now become economically viable. As a result, there are now many commercially available EM simulation software packages. From the user's point of view, these packages are of two types. The first type is the two-and-one-half dimensional (2.5-D) solver using planar surface meshing but including vertical currents between layers, useful for planar structures such as microstrips (vendors include SONNET, Zeland, Hewlett-Packard, Ansoft, and Compact Software). The second type is the full three-dimensional (3-D) solver using volume meshing, appropriate for truly 3-D problems (vendors include Hewlett-Packard, Ansoft, and MacNeal–Schwendler). The 2.5-D software is based on the method of moments while the 3-D software is based on finite-element analysis or finite-difference in the spectral domain. Only recently has finite-difference time-domain (FDTD) software become available [2]. At M/A-COM, the authors have extensively used Sonnet's em [3], Ansoft's Maxwell SI Eminence [20], and HP's HFSS [4] to design and optimize microwave (MW) circuits. In this paper, the efficient use of these commercial EM simulators for MW and millimeter-wave (MMW) circuit analysis and synthesis will be considered. It will be assumed that the reader is familiar with the details of the software usage and their features (such as line/plane of symmetry) and concentration will be on problem formulation and solution. Some of the material included in this paper has been presented in past workshops [12], [21].

Broadly speaking, there are three methods of using the commercially available EM simulators for MW and MMW circuit design. These are predictive characterization of circuit elements for use in larger circuits, optimization of circuit elements for circuit performance requirements, and creation of dimensionally scalable library elements for use in integrated circuit design and modeling. Fig. 1 illustrates the three methods together with the relationship of the various EM simulation tools to the circuit simulators. While all three methods generate data that is used in a circuit simulator, EM-based optimization may also do more EM simulations depending on the results of the circuit simulators.

Of the three categories, predictive characterization of circuit elements is usually the most accurate, easiest to accomplish, and requires the smallest amount of computer resources. This is achieved by careful isolation of the unknown structure from the known structures to reduce the problem size. For any EM simulation, it is very important to look ahead in terms of software requirements. The problem may have to be slightly modified, usually dimensionally, so that it is optimized for the software to be used; this can further reduce computation time. This issue will be discussed in some detail in Section II where
two examples of predictive characterization of discontinuities are demonstrated.

If the computed EM characteristics of the circuit element do not satisfy the overall circuit performance requirements, the geometry of the element needs to be modified. In such situations, numerous EM simulations are conducted to optimize the circuit element. In Section III, optimization of circuit elements using commercially available software is considered.

Circuit element optimization can be performed by either structural optimization or by dimensional optimization. Structural optimization refers to fundamental change in geometry, such as addition of new metal and dielectric patterns, while dimensional optimization refers to the modification of physical dimensions, such as length of a given metal and dielectric patterns. In Section III, structural optimization is first considered by utilizing various parameters such as field distribution, cross-coupling capacitors, and $S$-parameters and new structures for optimum performance are developed. Next, dimensional optimization is considered, where dimensions of a given structure are optimized. While parametrized and scalable equivalent circuits have been extensively used for dimensional optimization, recently, direct optimization using EM simulations has been demonstrated with improved optimization.
algorithms [5], [6]. A commercial software package, OSA’s Empipe [7], has UNIX-based links to Sonnet’s em to optimize a given structure using EM simulations. These new methods are efficient and examples of automatic circuit optimization using OSA’s Empipe will be given.

Even though the methods outlined above are capable of solving many MW problems, there are situations where circuit element building blocks are required for MW circuit design. Often these are accommodated in library wafer runs which are processed, measured, and modeled. However, as circuits are stressed to their performance limits, there is a continual need for process changes and novel circuit-element designs that improve circuit performance with improved yields. In a typical commercial environment, timely need for new library elements is most critical and often there is insufficient time for wafer runs to characterize new ideas. In such situations, a number of batch EM simulations are conducted—sometimes over a week or two—and dimensionally scalable library models are extracted. In Section IV, two examples of scalable circuit libraries are presented.

II. CHARACTERIZATION OF CIRCUIT ELEMENTS

In this section, a glass-based integrated circuit is first considered which shows how various elements in the circuit are characterized using EM simulations. The second example considers a surge protector for commercial frequencies illustrating predictive design to provide the required bandpass response. For reference, the glass microwave integrated circuit (GMIC) cross section is shown in Appendix I [8], [9].

Example 1—HMIC Switch Limiter: Fig. 2 shows the schematic for a matched 7–11 GHz single-pole double-throw (SPDT) switch in series with two stages of limiters. The bias of the diode labeled \( D_1 \) is tied to terminal 3 while that of \( D_2 \) is tied to terminal 4. Thus, when \( D_1 \) and \( D_2 \) are reverse biased and \( D_3 \) and \( D_4 \) forward biased, the signal from terminal 1 goes to terminal 3 while the signal from 2 is terminated in a high-power AlN resistor. The through path as well as the terminating path are simultaneously implemented as asymmetric commensurate line filters modified by capacitive loading [10], [11]. For the through path there is a shunt stub followed by two series quarter-wave sections and then a shunt
stub followed by another series section and a bias return shunt stub. Thus, the through path represents an order 4 filter while the terminating path is an order 2 filter; this is dictated by the circuit topology.

This circuit was implemented in heterolithic microwave integrated circuit (HMIC) technology [8], [15]. The p-i-n diodes marked $D_1$, $D_4$ are integrated in HMIC while the limiter p-i-n diodes marked $L_1$ and $L_2$ are chips bonded on the HMIC. The limiter diodes were not implemented in HMIC as the optimum I-region thickness required by the two limiter diodes are different from each other and from that of the integrated switch diodes $D_1$, $D_4$. The diodes have nonzero capacitance, which is incorporated in the filter using standard techniques [10], [11].

Fig. 3 shows the layout of the matched switch limiter as implemented in HMIC. The capacitors at terminals 1 and 2 were implemented by open-circuit stubs. The limiter diodes and the terminating AlN resistors are mounted on pedestals. The switch diodes are implemented in HMIC and have a well-controlled capacitance of 0.08 pF.

When the circuit was laid out in the allocated space, it was soon discovered that there were many circuit elements which were unknown and required characterization as they were critical for the circuit performance. In particular, the size forced the authors to bend lines outlined by the dashed boxes in Fig. 3 labeled A, D, and C, while loss forced us to use wide stubs as in box B instead of the inherently more lossy metal–insulator–metal (MIM) capacitors. Characteristics of these structures were inadequately represented in the linear circuit simulator and required EM simulations.

After the initial design using Hewlett-Packard’s circuit simulator MDS, a layout similar to, but dimensionally different from that in Fig. 3, was obtained by using the auto-layout functionality in MDS. Since Sonnet requires geometries to be defined on grid points, the authors’ initial designs were all adjusted for inclusion in Sonnet. Thus, the greatest common

<table>
<thead>
<tr>
<th>Resonant Frequency (GHz)</th>
<th>Measured</th>
<th>Simulated</th>
</tr>
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<tbody>
<tr>
<td>1.541</td>
<td>1.516</td>
<td></td>
</tr>
<tr>
<td>1.807</td>
<td>1.790</td>
<td></td>
</tr>
<tr>
<td>1.872</td>
<td>1.870</td>
<td></td>
</tr>
<tr>
<td>1.902</td>
<td>1.900</td>
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</tr>
<tr>
<td>1.917</td>
<td>1.911</td>
<td></td>
</tr>
<tr>
<td>2.035</td>
<td>2.047</td>
<td></td>
</tr>
<tr>
<td>2.107</td>
<td>2.136</td>
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Fig. 9. Table illustrates other designs and compares measured with simulated $F_o$. 

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Fig. 41. Future process enhancements that will require full 3-D EM simulation. These are required from commercial considerations of cost reduction with performance enhancement.

Step 4 may be clarified by recalling that the information is effectively replicated four times for the original array of inductors between pairs of ports. Connecting ports together or grounding them removes or combines some rows and columns while leaving undisturbed one of the original square

$Q$-factors are known, the corresponding parallel conductance can be accounted for as well.

Step 4. Isolate the proper submatrix and calculate its inverse. This yields an impedance matrix for the inductor array from which the resistance is obtained directly while the inductance is given by a fit over the desired frequency range to a straight line through the origin.

Fig. 42. GMIC cross section.

Fig. 43. $N$ mutually couple inductors.
submatrices which contains all the information remaining after the capacitances to ground are removed.

C. Application of the Technique to the 3-dB Backward Coupler

The circuit layout of the 3-dB backward coupler depicted in Fig. 27 was simulated in Sonnet. The $S$-parameters generated by Sonnet at 22, 24.5, 27, 29.5, and 32 GHz are first converted to $Y$-parameters.

On completion of Step 2 outlined above, a series combination of inductor and capacitor to ground is extracted at each port. The element values are forced to be symmetric by performing averaging to properly represent the electrical symmetry of the structure. Step 3 extracts the node-to-node capacitors, including series inductors where appropriate to better approximate distributed effects. These elements are also symmetrized as dictated by the circuit.

The remaining $Y$-matrix represents a coupled inductor pair. The impedance matrix is the matrix inversion of the proper isolated submatrix. The inductances are extracted by dividing the reactance by frequency, while losses are fitted to a linear function of frequency.

The extracted equivalent circuit is shown in Fig. 28. The calculated magnitude of the vector difference of the $S$-parameters generated by the equivalent circuit and that simulated by Sonnet for some of the pertinent $S$-parameters are shown in Fig. 44. The worst case error is less than 0.015 and the overall rms error is 0.008 supporting the accuracy of the extraction technique.

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REFERENCES


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